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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2671	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/895,777	DOYLE ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14,16-18 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14,16-18 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/27/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on December 27, 2005 was filed after the mailing date of the application on June 29, 2001. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

2. Applicant's arguments with respect to claims 1-12, 14, 16-18, and 20-27 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments, see pages 11-18, filed August 15, 2005, with respect to the rejection(s) of claim(s) 1-12, 14, 16-18, and 20-27 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Johns (US006674841B1).

4. Applicant argues that Flurry (US005455958A) and Potter (US006157393A) do not disclose a graphics-rendering engine to concurrently render two or more independent images for display on multiple display devices (page 12).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Johns.

5. Applicant argues that cited art Flurry doesn't teach that a second image with different data and being independent and distinct from the first image is displayed on the second display (page 13).

In reply, the Examiner argues that this is not claimed in Claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-3, 7-11, and 24, are rejected under 35 U.S.C. 103(a) as being unpatentable over Johns (US006674841B1) in view of Flurry (US005455958A).

9. With regard to Claims 1 and 24, Johns describes an apparatus, comprising a graphics-rendering engine (208, Figure 2) to render two or more independent images, the two or more independent images include a first independent image and a second independent image (*each application includes a graphic process, which generates graphics data for display*, Col. 4, lines 34-36; *first graphic application for producing a first graphical depiction...second graphics application for producing a second graphical depiction*, Col. 8, lines 15-20). Applications 300, 302, and 304 render graphics data for display by sending rendering command to FIFO 314 in graphics adapter 316 (Col. 4, lines 56-58). Device driver 306 does not have to wait for a context switch to complete before access to FIFO 314 is provided to another graphics process (Col. 4, lines 62-66). This means that while one application is rendering an image, another application can access the FIFO to render another image at the same time without waiting for a context switch to complete. This is the same problem that this invention is solving, according to the disclosure of this application (*graphics-rendering engine need not wait to completely process all of the instructions associated with the first independent image before starting to process instructions associated with the second independent image*, [0064]). Therefore, Johns discloses concurrently rendering two or more independent images; and a graphics context manager (rendering context management (RCM) 312, Figure 3; Col. 4, lines 40-44) to store in a first memory area and restore from the first memory area information describing a first rendering context associated with the first independent image, the graphics context manager to store in a second memory area and restore from the second memory area information describing a second rendering context associated with the second independent image (Col. 4, line 58-Col. 5, line 14; *context save command is sent with the context memory address to the adapter FIFO to save the*

current context to memory, Col. 6, lines 38-47). Johns describes that in the time sharing environment, each process has certain period of time of the hardware resource ownership (Col. 5, lines 26-28). The RCM controls when each process is allowed to access the graphics adapter (Col. 5, lines 28-47). Therefore, Johns inherently discloses a time allocator to arbitrate the use of the graphics-rendering engine between the two or more independent images, wherein the time allocator comprises a first module to establish a programmable elapsed period of time to use the graphics-rendering engine, the period of time is defined by a programmable number of unit time periods, where each unit time period is defined by a programmable number of real-time quanta (Col. 4, line 62-Col. 5, line 4; Col. 5, lines 22-47).

However, Johns does not teach that the images are for display on multiple display devices. However, Flurry describes a graphics-rendering engine (X Server program module 14, Figure 1; *as a display resource manager*, Col. 4, lines 14-44) to render two or more independent images for display on multiple display devices (*this invention is designed to function with several display devices connected to it*, Col. 5, lines 25-30).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Johns so that the images are for display on multiple display devices as suggested by Flurry because the images can be viewed by several different users (Col. 5, lines 16-19, 25-30).

10. With regard to Claim 2, Johns describes that the graphics context manager saves context in memory by sending a context save command with the context memory address to the adapter FIFO (Col. 6, lines 38-47). Since the each context is saved at a specific memory address in the

system memory (Col. 6, lines 41-43), Johns inherently discloses that the graphics context manager further comprises a plurality of memory areas in the system memory, each memory area in the system memory to store a rendering context associated with the instructions from a particular graphics application (300, 302, 304, Figure 3), the plurality of memory areas in the system memory includes the first memory area and the second memory area (Col. 6, lines 38-47). According to the disclosure of this application, the plurality of memory areas that store the rendering contexts are in system memory (*rendering contexts associated with a specific graphics application may be stored in multiple established memory locations 216, 218, 220 in system memory 232,* [0034]), and this is also what Johns teaches. Johns also describes a plurality of context identification registers (318) including a first context identification register and a second context identification register, the first context identification register contains information to point to an address of the first memory area, the second context identification register contains information to point to an address of the second memory area (Col. 4, line 58-Col. 5, line 14; Col. 6, lines 38-47).

11. With regard to Claim 3, Johns does not explicitly disclose a third register to track which memory area in the plurality of memory areas contains the rendering context information to be supplied to the graphics-rendering engine. However, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to include such a register because it would improve the efficiency of rendering context manager.

12. With regard to Claim 7, Johns describes the first memory area to contain instructions for the two or more independent images in a first instruction stream (*applications 300, 302, and 304 render graphics data for display by sending rendering commands to FIFO 314, RCM request a device driver to send context switch commands to the same FIFO*, Col. 4, line 58-Col. 5, line 14; Col. 6, lines 38-47).

13. With regard to Claim 8, Claim 8 is similar in scope to Claim 7, and therefore is rejected under the same rationale.

14. With regard to Claim 9, Claim 9 is similar in scope to Claim 7, and therefore is rejected under the same rationale.

15. With regard to Claim 10, Johns describes that each instruction transport (312, Figure 3) is associated with a particular display device (210, Figure 2) (Col. 4, lines 40-50; *graphics adapter 208 processes graphics data for display on display device 210*, Col. 3, lines 57-58).

16. With regard to Claim 11, Johns describes that the first instruction transport comprises an instruction memory area (314, Figure 3; Col. 4, lines 56-58); and a memory access engine to fetch and deliver the instructions from the instruction memory area to the graphics-rendering engine (*the FIFO is restored from memory to the adapter*, Col. 6, lines 16-19).

However, Johns does not explicitly teach a first register to define a start and an end to the instruction memory area. However, Johns describes that the FIFO is saved from the adapter to

memory (Col. 6, lines 14-19), and therefore it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to include such a register because it would improve the efficiency of rendering context manager.

17. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johns (US006674841B1) and Flurry (US005455958A) in view of Puar (US005703806A).

Johns and Flurry are relied upon for the teachings as discussed above relative to Claim 1.

However, Johns and Flurry do not teach that the first memory area is located on the same chip containing the graphics-rendering engine. However, Puar describes a graphics controller function being integrated on the same chip as the memory (Col. 2, lines 58-67).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Johns and Flurry so that the first memory area is located on the same chip containing the graphics-rendering engine because it provides for low power consumption, and low pin and package counts thus resulting in cost savings.

18. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johns (US006674841B1) and Flurry (US005455958A) in view of Kohli (US006252600B1).

19. With regard to Claim 5, Johns and Flurry are relied upon for the teachings as discussed above relative to Claim 2.

However, Johns and Flurry do not teach a two dimensional and three dimensional image being processed. However, Kohli describes a graphics context management arrangement that

involves two dimensional and three dimensional image processing (Col. 4, lines 46-67; Figure 3).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Johns and Flurry to include a two dimensional and three dimensional image being processed as suggested by Kohli. Kohli suggests that increasingly, computer graphics systems are supporting multiple 2D and 3D contexts. For example, a graphics system may have in one window a high quality rendering of an airplane being developed. In another window there may be an interactive dialog in which the designer can change the properties of the airplane or make inquiries about it (Col. 1, lines 46-55). Fast context switching is needed (Col. 2, lines 35-40) so that a user does not need to wait for a 2D window to display while a high quality 3D rendering is being developed in another window (Col. 2, lines 14-27).

20. With regard to Claim 6, a textured-map image is similar to a 3D image and a non-texture-mapped image is similar to a 2D image, and therefore Claim 6 is similar to Claim 5, and therefore is rejected under the same rationale. It would be obvious to switch from a textured-map context to a non-texture-mapped context for the same reasons for switching from a 3D context to a 2D context, which are discussed in the rejection for Claim 5.

21. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johns (US006674841B1) and Flurry (US005455958A) in view of Rogers (US004530047A).

Johns and Flurry are relied upon for the teachings as discussed above relative to Claim 9.

However, Johns and Flurry do not teach that the instruction transport further comprises a third memory area to store an independent sequence of instructions that can be invoked from an instruction stream. According to the disclosure of this application, this third memory area is a batch buffer that contains a separate list of image rendering instructions that may be stored in a discrete memory area to provide extra instruction storage capacity [0020]. Rogers describes a third memory area for additional storage of instructions that can be invoked from an instruction stream (Col. 3, lines 45-48; Col. 35, lines 7-17).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Johns and Flurry so that the instruction transport further comprises a third memory area to store an independent sequence of instructions that can be invoked from an instruction stream as suggested by Rogers because Rogers suggests that if the instruction memory area runs out of memory, processing can continue by accessing the instructions from the third memory area, and this is useful for simultaneously processing operations (Col. 3, lines 43-58).

22. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johns (US006674841B1) and Flurry (US005455958A) in view of Mills (US006311204B1).

23. With regard to Claim 14, Johns and Flurry are relied upon for the teachings as discussed above relative to Claim 1.

However, Johns and Flurry do not teach that the time allocator comprises a plurality of registers including a first register, the first register having a plurality of fields, a first field to

determine whether the first register participates in an arbitration process to use the graphics rendering engine, a second field to point to a memory location containing instructions from a first instruction stream. However, Mills describes a processing system with register-based process sharing. The acquire bit portion (352, Figure 9A) of the semaphore register 350 indicates other processes when it engages the drawing acceleration engine similar to the instant claim where a first field indicates whether the first register will participate in using the graphics engine (Col. 27, lines 18-63). The process identifier portion 354 of the semaphore register 350 can be made to point to a memory location for fetching instructions from a first instruction stream. This is not explicitly disclosed, but such operation falls within the realm of fetching instructions being pointed to by a process identifier portion of the semaphore register.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Johns and Flurry so that the time allocator comprises a plurality of registers including a first register, the first register having a plurality of fields, a first field to determine whether the first register participates in an arbitration process to use the graphics rendering engine, a second field to point to a memory location containing instructions from a first instruction stream as suggested by Mills because this would result in improved efficiency and reduce cost and complexity.

24. With regard to Claim 16, wherein a first module directs the graphics-rendering engine to process instructions stored in a first memory having an address defined by information contained in the plurality of fields, this is implicitly taught by Mills as described above (*fetching*

instructions being pointed to by a process identifier portion of the semaphore register, Col. 27, lines 18-63).

25. Claims 17, 18, 20-23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johns (US006674841B1) in view of Dye (US006002411A).

26. With regard to Claim 17, Johns describes that the applications 300, 302, and 304 send rendering commands to the FIFO (Col. 4, lines 56-58), and the FIFO receives the commands continuously with no wait period (Col. 8, lines 22-24), and therefore the concurrent rendering instructions associated with multiple independent images are within a first instruction-stream (Col. 4, lines 34-36, 56-66; Col. 8, lines 15-20); storing in a first memory area information representing a first rendering context associated with a first independent image; restoring from a second memory area instructions representing a second rendering context associated with a second independent image, wherein the first memory area and the second memory area are included in a plurality of memory areas; switching the first rendering context to the second rendering context (Col. 4, line 58-Col. 5, line 14; Col. 6, lines 38-47).

However, Johns does not teach using a volatile memory device to track which memory area in the plurality of memory areas contains the rendering context information to be supplied to a graphics-rendering engine. However, Dye describes a volatile memory device to track which memory area in the plurality of memory areas contains the rendering context information to be supplied to a graphics-rendering engine (Col. 23, line 66-Col. 24, line 10). This would be obvious for the same reasons given in the rejection for Claim 27.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Johns to include using a volatile memory device to track which memory area in the plurality of memory areas contains the rendering context information to be supplied to a graphics-rendering engine as suggested by Dye because Dye suggests that it would improve the efficiency of rendering context manager (Col. 23, line 66-Col. 24, line 10).

27. With regard to Claim 18, Johns describes using a timing circuit to allocate the use of the graphics-rendering engine between instructions associated with the first graphics application and instructions associated with the second graphics application (Col. 4, line 62-Col. 5, line 4; Col. 5, lines 22-47).

28. With regard to Claim 20, Johns describes displaying the multiple independent images on a single display device (210, Figure 2) (Col. 3, lines 57-58; Col. 4, lines 34-36, 56-66; Col. 8, lines 15-20).

29. With regard to Claim 21, Claim 21 is similar in scope to Claim 17, and therefore is rejected under the same rationale.

30. With regard to Claim 22, Johns describes that the graphics device further comprises a time allocator to arbitrate the use of the graphics-rendering engine between the two or more independent images (Col. 4, line 62-Col. 5, line 4; Col. 5, lines 22-47).

31. With regard to Claim 23, Johns describes that the graphics device further comprises an instruction transport to deliver instructions for the independent images to the graphics-rendering engine as controlled by the time allocator (Col. 4, line 62-Col. 5, line 4; Col. 5, lines 22-47).

32. With regard to Claim 26, Johns describes converting a variety of time specifying parameters in the instructions in the first instruction stream into real-time periods of use of the graphics-rendering engine (Col. 4, line 58-Col. 5, line 14; Col. 5, lines 22-47).

33. Claim 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Johns (US006674841B1) and Flurry (US005455958A) in view of Dye (US006002411A).

Johns and Flurry are relied upon for the teachings as discussed above relative to Claim 1. Johns describes saving the rendering context information to be supplied to the graphics-rendering engine in memory at a context memory address (Col. 6, lines 36-43). Johns also describes receiving instructions from a graphics application (300, 302, 304, Figure 3) generating instructions for one or more of the independent images (Col. 4, lines 56-58).

However, Johns does not explicitly teach using tracking registers to track this. However, Dye describes a tracking register to track which memory area contains the rendering context information to be supplied to the graphics-rendering engine (Col. 23, line 66-Col. 24, line 10) independently of the tracking register receiving instructions (Col. 15, lines 34-35). This would be obvious for the same reasons given in the rejection for Claim 17.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

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